Q.P. Code: 16EC431 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech IV Year I Semester Supplementary Examinations February-2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Explain the steps involved in fabrication of a p-well process CMOS transistor.	**7M**
	b	List steps involved in n-well process.	**5M**
		OR	
2		Determine the relationship between I_{ds} & V_{ds} in non-saturated and saturated region.	**12M**

UNIT-II

3	a	Discuss the lambda-based design rules with neat sketches.	**6M**
	b	What is a stick diagram? Design the stick diagram of a three input CMOS NAND gate.	**6M**
		OR	
4	a	Explain how the p-MOS transistor forms in lambda-based design rules.	**6M**
	b	Design the layout diagram for CMOS inverter?	**6M**

UNIT-III

5	a	What is switch logic?	**4M**
	b	Illustrate the dynamic CMOS logic circuit with any one example.	**8M**
		OR	
6	a	Explain how the clock and power distributions employed in VLSI design circuits with diagrams.	**6M**
	b	Illustrate the Power delay estimation in VLSI circuits.	**6M**

UNIT-IV

7	a	What is shifter? List the types of shift registers.	**6M**
	b	Design and explain the shifter implemented by using full adder.	**6M**
		OR	
8	a	Explain about 4 transistor Dynamic memory cell.	**6M**
	b	Explain the 6 transistor Static memory cell.	**6M**

UNIT-V

9	a	Design and explain the architecture of FPGA.	**6M**
	b	Discuss the merits of FPGA over other architectures.	**6M**
		OR	
10	a	What is the need for testing? And explain about Fault simulation.	**6M**
	b	Explain about design strategies for testing.	**6M**

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